REMARKS

Claims 1 and 3-21 are pending. Claims 1, 7, and 15 are independent claims. Reconsideration and allowance of the above-referenced application are respectfully requested.

Non-statutory Double Patenting

Claims 1 and 3-21 stand rejected on the ground of non-statutory obviousness-type double patenting as allegedly being unpatentable over claims 1-17 of Adiletta et al. (U.S. Patent No. 6,606,704), hereinafter "Adiletta."

A terminal disclaimer, in compliance with 37 CFR 1.321, is filed with this response to overcome the double patenting rejection.

35 USC 103

Claims 1 and 3-21 stand rejected under 35 USC 103(a) as allegedly being unpatentable over Kahle et al. (US 6,212,542), hereinafter "Kahle" in view of Belkin (US 6,604,125), hereinafter "Belkin." The rejections are respectfully traversed. The hypothetical combination of Kahle and Belkin do not describe or suggest all the features of the claimed subject matter.

Kahle describes a multi-scalar processor and method of executing a multi-scalar program within a multi-scalar processor having a plurality of processing elements and a thread scheduler. See, e.g., Kahle at Abstract. Kahle does not describe or suggest all the features of claim 1.

In this regard, Kahle states:

> According to the method, a third data structure among the plurality of data structures is supplied to the thread scheduler. The third data structure, which is associated with a third thread among the plurality

> of threads, specifies a first data structure associated with a first possible exit point of the third thread and a second data structure associated with a second possible exit point of the third thread. The third thread is assigned to a selected one of the plurality of processing elements for execution. Prior to completing execution of the third thread, the thread scheduler selects from among the first and second possible exit points of the third thread. In response to the selection, a corresponding one of the first and second data structures is loaded into the thread scheduler for processing. (Emphasis added).

See, Kahle, Abstract.

Thus, Kahle describes that the thread scheduler selects from among the first and the second possible exit points of the third thread prior to completing execution of the third thread, and loads a corresponding data structure into the thread scheduler for processing.

With respect to claim 1, the cited portions of Kahle (Kahle, abstract, figures 4 and 6, and the corresponding description thereof) do not describe or suggest scheduling a first thread to process a first incoming block of data within a network packet, and scheduling a second thread to process a second incoming block of data within the network packet prior to the first thread completing processing of the first incoming block of data, as described in claim 1.

Belkin does not rectify these deficiencies in Kahle. Belkin describes enabling a thread unaware application to be executed safely in a multi-threaded environment. See, Belkin at Abstract. Belkin does not describe or suggest "scheduling a first thread provided by the multiple programmable multi-threaded engines integrated within the processor to process a first incoming block of data within a network packet received at port of a media access control device, and scheduling a second thread provided by the multiple programmable multi-threaded

engines integrated within the processor to process a second incoming block of data within the network packet prior to the first thread completing processing of the first incoming block of data," as recited in claim 1.

Thus, neither Kahle nor Belkin, taken alone or in combination describe or suggest the features of claim 1. Therefore, a *prima facie* case of obviousness is not established. Accordingly, claim 1 is patentable.

Claims 3-6 and 18-20 are also patentable at least for reasons similar to claim 1 and for the additional recitations that they contain.

Claim 7 is patentable for reasons similar to claim 1. Claims 8-14 and 21 are also patentable at least for similar reasons and for the additional recitations that they contain.

Claim 15 is patentable for reasons similar to claim 1. Claims 16 and 17 are also patentable at least for similar reasons and for the additional recitations that they contain.

CONCLUSION

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicant asks that all claims be allowed. Please apply any credits or charges to deposit account 06-1050.

Respectfully submitted,

Date: 7/18/07

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